REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-21 in the application. In a previous response, the Applicants amended Claims 1, 8, and 15 with limitations from Claims 5, 12, and 19, respectively, and canceled Claims 5, 12, and 19 without prejudice or disclaimer. In the present response, the Applicants have not amended, canceled, or added any claims. Accordingly, Claims 1-4, 6-11, 13-18, and 20-21 are currently pending in the application and in condition for allowance.

I. Rejection of Claims 1 and 8 under 35 U.S.C. §102

The Examiner has rejected Claims 1 and 8 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,079,860 to Yamamoto, *et al.* The Applicants respectfully disagree.

Yamamoto discloses an embodiment of a LNA including a source inductor 221 connected between a source of a first FET1 201 and a second FET2 202 and a constant current source 115. (*See* column 14, lines 30-32 and Figure 12.) The Applicants fail to find where Yamamoto teaches the source inductor 221 is configured to resonate proportionally to a frequency of received signals with a first capacitance associated with the first FET1 201 and second FET2 202. On the contrary, Yamamoto teaches the source inductor 221 is used to improve the stability factor of the two FETs 201 and 202 while ensuring a desirable gain of the first and second FETs 201 and 202, thereby achieving both a low noise figure and a desirable input return loss in the FETs 201 and 202. (*See* column 14, lines13-19, lines 37-39, and Figures 10 and 12.) Additionally, Yamamoto teaches the value of the source inductor 221 is determined so as to ensure that the gain of the FET whose input signal has the higher frequency is at an appropriate value. (*See* column 14, lines 10-12, lines 37-39 and Figures 10 and 12.)

Thus, Yamamoto teaches that the inductor is configured to ensure the gain of the FET of the LNA whose input signal has the higher frequency is at an appropriate value to achieve a low noise figure and a low input return loss. Yamamoto does not teach that the inductor is configured to resonate proportionally to a frequency of received signals with a first capacitance associated with the plurality of transistors. As such, Yamamoto does not teach each and every element of independent Claims 1 and 8 and, therefore, does not anticipate independent Claims 1 and 8 and Claims that depend thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102(e) rejection of Claims 1 and 8 and allow issuance thereof.

II. Rejection of Claims 2-4, 6, 7, 9-11, 13-18, and 20-21 under 35 U.S.C. §103

The Examiner has rejected Claims 2-4, 6, 7, 9-11, 13-18, and 20-21 under 35 U.S.C. §103(a) as being unpatentable over Yamamoto in view of U.S. Patent No. 5,884,154 to Sano, *et al.* The Applicants respectfully disagree.

As established above, Yamamoto does not teach an inductor, coupled between a common source of a plurality of transistors and a current generator, configured to resonate proportionally to a frequency of received signals with a first capacitance associated with the plurality of transistors as recited in independent Claims 1 and 8. Furthermore, Yamamoto does not suggest the same.

Yamamoto relates to reducing the number of components in a high frequency block of a dual-band portable telephone so as to realize a reduction in the size of the dual-band portable telephone. (*See* column 2, lines 64-67.) The dual-band portable phone requires at least two low noise amplifiers (LNA) in the high frequency block of the dual-band portable phone. To help realize the objective of Yamamoto to reduce size, the LNAs are combined in a single circuit 117. (*See*

Figures 1, 10, and 12.) The LNAs of Yamamoto are implemented with FETs, which are combined in the single circuit 117. Yamamoto uses, for example, the source inductor 221 to optimize the characteristics of the FETs in the LNA with regard to maximizing gain and reducing noise. One of ordinary skill in the art at the time of the invention would not be motivated to configure the inductor of Yamamoto to resonate proportionally to the frequency of the received signals of the LNA with a first capacitance associated with the FETs of the LNA as presently claimed, since this configuration would not provide the desired optimized gain and noise performance of the FETs in the LNA of Yamamoto. As such, Yamamoto does not establish a *prima facie* case of obviousness of independent Claims 1 and 8, and analogously, independent Claim 15, and Claims that depend thereon.

The Examiner does not cite Sano to cure the deficiency of Yamamoto but to teach the subject matter of dependent Claims 2-4, 6-7, 9-11, 13-14, 16-18, and 20-21 and to teach other limitations of independent Claim 15. (*See* Examiner's Action electronically delivered April 20, 2007, pages 3-6.) Additionally, the Applicants do not find where Sano cures the deficiency of Yamamoto. As such, the cited combination of Yamamoto and Sano does not establish a *prima facie* case of obviousness of independent Claims 1, 8, and 15 and Claims that depend thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of Claims 2-4, 6-7, 9-11, 13-18, and 20-21 and allow issuance thereof.

III. Conclusion

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-4, 6-11, 13-18, and 20-21.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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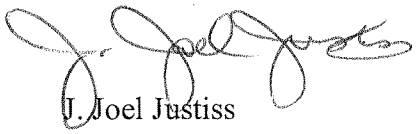

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